IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	Azadet et al
Case:	14-6
Serial No.:	10/022,659
Filing Date:	December 18, 2001
Group:	2611
Examiner:	Juan A. Torres

Title: Method and Apparatus for Joint Equalization and Decoding of Multilevel Codes

---

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby appeal the final rejection dated March 2, 2007, of claims 1, 2, 7-10, 12, and 15-29 of the above-identified patent application

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc., as evidenced by an assignment recorded on December 18, 2001 in the United States Patent and Trademark Office at Reel 012396, Frame 0222. The assignee, Agere Systems Inc., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-2, 7-10, 12, and 15-29 are presently pending in the above-identified patent application. Claims 16-19 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan (United States Patent No. 6,418,172) in view of Trans (United States Patent No. 6,377,640). Claims 1, 7, 8, 12, and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of "A Low Complexity Joint Equalizer and Decoder for 1000 Base-T Gigabit Ethernet" (Haratsch 1). Claim 20 is rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Trans, and further in view of Haratsch 1. Claims 2, 9, 10 and 23-29 are rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan and Haratsch 1 and further in view of "High Speed VLSI Implementation of Reduced Complexity Sequence Estimation Algorithms with Application to Gigabit Ethernet 1000Base-T" (Haratsch 2). Claims 1, 8, 16, 26, and 29 are being appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a method for decoding a signal received from a dispersive channel causing intersymbol interference, the signal encoded using an MLT-3 code, the method comprising the steps of: generating at least one trellis representing both the MLT-3 code and the dispersive channel (page 4, line 11, to page 5, line 8); and performing joint equalization and decoding of the received signal using the trellis (page 5, lines 10-21; page 6, lines 9-21).

Independent claim 8 is directed to a receiver for processing a signal received from a dispersive channel, the signal encoded using an MLT-3 code, comprising: a sequence detector that performs joint equalization and decoding of the received signal using at least one trellis representing both the MLT-3 code and the dispersive channel (page 5, lines 10-28).

Independent claim 16 is directed to a method for representing an MLT-3 code as a trellis, the MLT-3 code using three signal levels to represent two binary values, the method comprising the steps of: generating the trellis with a plurality of trellis states, each of the trellis states associated with a value for a signal in a previous symbol period (page 4, lines 10-22); and generating each of the trellis states with at least two branches leaving or entering each state, each of the at least two branches corresponding to state transitions associated with the two binary values, wherein a first binary value substantially always causes a state transition in the trellis from a first state to a different state and a second binary value does not cause a state transition in the trellis (page 4, lines 10-22); and using the trellis to decode a signal encoded using the MLT-3 code (page 5, lines 10-28).

In one exemplary embodiment, a number of states in the trellis is given by $4x(2^K)$, where K is the truncated channel memory (page 6, lines 9-21).

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 16-19 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Trans. Claims 1, 7, 8, 12, and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Haratsch 1. Claims 2, 9, 10 and 23-29 are rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan and Haratsch 1 and further in view of Haratsch 2.

ARGUMENT

Independent Claim 16

Independent claim 16 was rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Trans. The Examiner asserts that Raghavan discloses a method for representing an MLT-3 code as a trellis using three signal levels to represent two binary values, the method comprising generating the trellis with a plurality of trellis states, each of the trellis states associated with a value for a signal in a previous symbol period; and generating each of the trellis states with at least two branches leaving or entering each state, each of the at least two

branches corresponding to state transitions associated with the two binary values.

Appellants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness for at least the reason that there exists no motivation to combine the references, and further, even if combinable, the references collectively do not teach each and every limitation of the independent claims. See, e.g., M.P.E.P. §2143.

The Examiner acknowledges that Raghavan does not disclose that a first binary value substantially always causes a *state transition in said trellis* from a first state to a different state and a second binary value does not cause a *state transition in said trellis*," as required by claim 16. The Examiner asserts, however, that this feature is shown by Trans. As previously asserted by Appellants, however, (but **not** addressed by the Examiner at all in the Response to Arguments section of the latest Office Action), Trans teaches that each time a logic "1" is encoded, a transition (equal to an output value transition) will take place (there is no mention of causing a state transition in a trellis). Likewise, each time a logic 0 is encoded, the previous output level will be maintained for another bit period (again, there is no mention of causing a state transition in a trellis). See, Col. 61, lines 48-56. Trans does not disclose representing an MLT-3 code using a trellis, and thus, states or state transitions are not defined in Trans, as those terms are used by the present invention.

As asserted in Appellants' prior responses, Raghavan discloses that a binary logic one (1) is transmitted as either a -1 or +1, and a binary logic zero (0) is transmitted as a 0 (see, col. 1, lines 24-36 and FIG. 1A). Thus, in Raghavan (for example, Fig 1A), the input value 1 *sometimes* causes a transition into the same state, and sometimes a transition into a different state. Thus, one value does not always lead to a state transition as defined in claim 16.

Raghavan thus teaches away from using Trans to achieve what is claimed by the present invention, as Raghavan does not define state transitions in the manner required by claim 16. *Compare,* the trellis of Raghavan to the MLT- trellis of the present invention. This "teaching away" is contrary to the combination suggested by the Examiner, even if both references are in the same field of endeavor (Ethernet communications).

Further, even if combinable, the references *collectively* do not teach each and every limitation of the independent claims. As indicated above, Trans does not disclose representing an MLT-3 code using a trellis, and thus, states or state transitions are not defined in Trans, as those terms are used by the present invention. Rather, Trans teaches that each time a logic "1" is encoded, a transition (equal to an output value transition) will take place (there is no mention of causing a state transition in a *trellis*). Likewise, each time a logic 0 is encoded, the previous output level will be maintained for another bit period (again, there is no mention of causing a state transition in a *trellis*). See, Col. 61, lines 48-56.

Thus, Raghaven and Trans, alone or in combination, do not disclose or suggest "generating each of said trellis states with at least two branches leaving or entering each state, each of said at least two branches corresponding to state transitions associated with said two binary values, wherein a first binary value *substantially always* causes a state transition in said trellis *from a first state to a different state* and a second binary value does not cause a state transition in said trellis," as required by claim 16.

Independent Claims 1 and 8

Independent claims 1 and 8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Haratsch 1. Regarding claims 1 and 8, the Examiner asserts that Raghavan discloses MLT-3 encoding. The Examiner acknowledges that Raghavan does not disclose decoding a signal received from a dispersive channel causing intersymbol interference comprising generating at least one trellis representing the code and the dispersive channel; and performing joint equalization and decoding of the received signal using the trellis. The Examiner asserts, however, that this feature is shown by Haratsch 1.

Appellants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness, for at least the reason that there exists no motivation to combine the references. See, e.g., M.P.E.P. §2143. First, as asserted in Appellants' prior responses, MLT-3 codes are not trellis coded modulation (TCM) as described by Haratsch 1. Thus, it would not be obvious to a person of ordinary skill in the art to generate a trellis representing the MLT-3 and dispersive channel, in the manner suggested by the present invention.

Furthermore, Haratsch 1 is addressing *four dimensional* TCM codes with 8 states. Thus, the corresponding computations disclosed by Haratsch 1, such as the branch metric computations, do not make sense in the context of the present invention. For example, Equations 1 and 2 of Haratsch 1 do not make sense for MLT-3 codes, as they show the computation of the 1D ISI estimates and 1D branch metrics for each of the 4 dimensions. Page 466, left column, then shows how to combine the 1D branch metric to obtain 4D branch metrics for the 4D TCM code, which again does not make sense for MLT-3 codes. See also Figures 2 and 4, where one and four dimensional branch metric units are shown.

In addition, as discussed hereinafter, if the combination was attempted in the manner suggested by the Examiner, an expression is obtained for the number of states that does not make sense. The number of trellis states in Haratsch 1 is equal to the number of TCM code states and therefore equal to 8. In the present invention, on the other hand, the number of trellis states is $4x(2^K)$, where K is the truncated channel memory.

These incompatibilities between the combination of Raghavan/Haratsch 1 is contrary to the combination suggested by the Examiner, even if both cited references are in the same field of endeavor (Ethernet communications). Thus, a person of ordinary skill in the art would not make such a combination.

In addition to providing a different number of states, which suggests away from the combination, the minimum number of states associated with the present invention ($4x(2^K)=4$ for K=0) is lower than Haratsch 1. This is a "*surprising result*" which is further evidence of non-obviousness. This was **not** addressed by the Examiner in the Response to Arguments section of the latest Office Action.

Furthermore, the Examiner asserts that the motivation for combining Raghavan with Haratsch 1 would be to reduce the complexity of the system. Rather, claims 1 and 8 in fact generally increase the complexity of the system (joint equalization and decoding using a trellis representing both the MLT-3 code and dispersive channel) compared to a prior art system with a MLT-3 decoder and separate equalizer.

Claims 26 and 29

With respect to claims 26 and 29, for example, the Examiner asserts that Haratsch 2 discloses that the number of states in the trellis is given by $4x(2^K)$, where K is the truncated channel memory. (citing page 171) In the passage of Haratsch 2 recited by the Examiner, however, the number of states is given by $Sx(2^{mL})$, where S is the number of TCM code states, m the number of bits that are fed into the TCM encoder, and L is the (full) channel memory m is defined in Fig.2 of Haratsch 2 for TCM codes, but is undefined for MLT-3 codes, which are different from TCM codes. Significantly, the equation in page 171 of Haratsch 2 uses the channel memory L, while claims 26 and 29 use the truncated channel memory K. Therefore, the equation in page 171 of Haratsch 2 is different and undefined for MLT-3 codes. This was **not** addressed by the Examiner in the Response to Arguments section of the latest Office Action

Dependent Claims

Claims 2, 7, 9-10, 12, 15 and 17-29 are dependent on claims 1, 8, or 16, and are therefore patentably distinguished over Raghavan, Haratsch 1, Trans, and Haratsch 2 (alone or in any combination) because of their dependency from independent claims 1, 8, and 16 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

Conclusion

The rejections of the cited claims under section 103 in view of Raghavan, Haratsch 1, Trans, and Haratsch 2, alone or in any combination, are therefore believed to be improper and should be withdrawn. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,

Date: August 13, 2007

Kevin M. Mason
Attorney for Applicant(s)
Reg. No. 36,597
Ryan, Mason & Lewis, LLP
1300 Post Road, Suite 205
Fairfield, CT 06824
(203) 255-6560

CLAIMS APPENDIX

1. A method for decoding a signal received from a dispersive channel causing intersymbol interference, said signal encoded using an MLT-3 code, said method comprising the steps of:

generating at least one trellis representing both said MLT-3 code and said dispersive channel; and

performing joint equalization and decoding of said received signal using said trellis.

2. The method of claim 1, wherein said performing step uses a reduced complexity sequence estimation technique.

3. (Cancelled).

4. (Cancelled).

5. (Cancelled)

6. (Cancelled).

7. The method of claim 1, wherein said dispersive channel is an Ethernet channel.

8. A receiver for processing a signal received from a dispersive channel, said signal encoded using an MLT-3 code, comprising:

a sequence detector that performs joint equalization and decoding of said received signal using at least one trellis representing both said MLT-3 code and said dispersive channel.

9. The receiver of claim 8, wherein said sequence detector employs a reduced complexity sequence estimator.

10. The receiver of claim 9, wherein said reduced complexity sequence estimator employs a reduced-state trellis having a reduced number of states, wherein said reduced complexity sequence estimator further comprises:

a branch metric units (BMU) that calculates branch metrics based on said received signal;

an add-compare-select unit (ACSU) that determines the best surviving paths into said reduced states;

a survivor memory unit (SMU) that stores said best surviving paths; and

a decision-feedback unit (DFU) that takes survivor symbols from said SMU to calculate ISI estimates for said reduced states, wherein said ISI estimates are used by said BMU to calculate branch metrics for transitions in the reduced-state trellis.

11. (Cancelled).

12. The receiver of claim 8, wherein said sequence detector further comprises:

a branch metric units (BMU) that calculates branch metrics based on said received signal;

an add-compare-select unit (ACSU) that determines the best surviving paths into said trellis states; and

a survivor memory unit (SMU) that stores said best surviving paths.

13. (Cancelled).

14. (Cancelled).

15. The receiver of claim 8, wherein said dispersive channel is an Ethernet channel

16. A method for representing an MLT-3 code as a trellis, said MLT-3 code using three signal levels to represent two binary values, said method comprising the steps of:

generating said trellis with a plurality of trellis states, each of said trellis states associated with a value for a signal in a previous symbol period; and

generating each of said trellis states with at least two branches leaving or entering each state, each of said at least two branches corresponding to state transitions associated with said two binary values, wherein a first binary value substantially always causes a state transition in said trellis from a first state to a different state and a second binary value does not cause a state transition in said trellis; and

using said trellis to decode a signal encoded using said MLT-3 code.

17. The method of claim 16, wherein a first one of said plurality of trellis states corresponds to a value for a signal in a previous symbol period of +1.

18 The method of claim 16, wherein a second and third of said plurality of trellis states corresponds to a value for a signal in a previous symbol period of 0.

19. The method of claim 16, wherein a fourth one of said plurality of trellis states corresponds to a value for a signal in a previous symbol period of -1.

20. The method of claim 16, further comprising the step of using said trellis to perform joint equalization and decoding of a signal encoded using said MLT-3 code.

21. The method of claim 16, further comprising the step of combining said trellis with a trellis representing a channel to obtain a super trellis.

22. The method of claim 16, wherein said dispersive channel is an Ethernet channel.

23. The method of claim 1, wherein a state in said trellis is given by a concatenation of said MLT-3 code state and a channel state, wherein said channel state describes said dispersive channel

24. The method of claim 1, wherein a state in said trellis is given by a concatenation of said MLT-3 code state and a truncated channel state, wherein said truncated channel state partially describes said dispersive channel

25. The method of claim 24, further comprising the steps of computing ISI estimates for said states using symbols from corresponding survivor paths; computing branch metrics for transitions in said trellis based on said ISI estimates; determining survivor paths into said states based on said branch metrics; and storing said survivor paths.

26. The method of claim 24, wherein a number of states in said trellis is given by $4x(2^K)$, where K is the truncated channel memory.

27. The receiver of claim 8, wherein a state in said trellis is given by a concatenation of said MLT-3 code state and a channel state, wherein said channel state describes said dispersive channel.

28. The receiver of claim 8, wherein a state in said trellis is given by a concatenation of said MLT-3 code state and a truncated channel state, wherein said truncated channel state partially describes said dispersive channel.

29. The receiver of claim 28, wherein a number of states in said trellis is given by $4x(2^K)$, where K is the truncated channel memory.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to § 1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by appellant

RELATED PROCEEDINGS APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37